JW5018

40V/600mA, 2MHz Synchronous Step-Down Converter

DESCRIPTION

The JW®5018 is a current mode monolithic buck switching regulator. Operating with an input range of 4.7V~40V, the JW5018 delivers 600mA of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, the regulator operates in low frequency to maintain high efficiency and low output ripple. Current mode control provides tight load transient response and cycle-by-cycle current limit.

The JW5018 guarantees robustness with short-circuit protection, thermal protection, current run-away protection, and input under voltage lockout.

The JW5018 is available in 6-pin SOT23-6 package, which provides a compact solution with minimal external components.

FEATURES

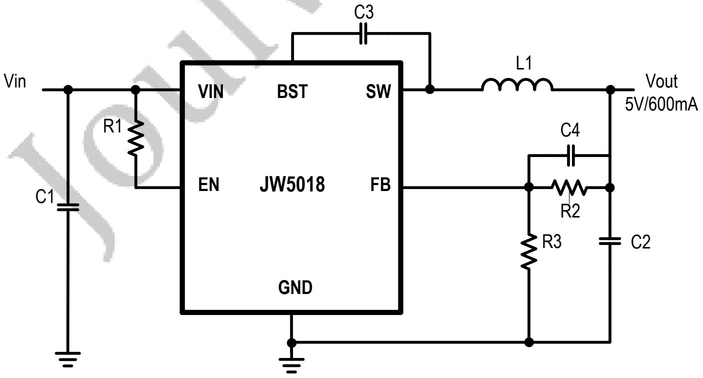
- 4.7V to 40V operating input range 600mA output current
- Up to 93% efficiency
- High efficiency (>78%) at light load
- Internal soft-start
- Up to 96% duty cycle
- 2MHz switching frequency
- Input under voltage lockout
- Current run-away protection
- Short circuit protection
- Thermal protection
- Available in SOT23-6 package

APPLICATIONS

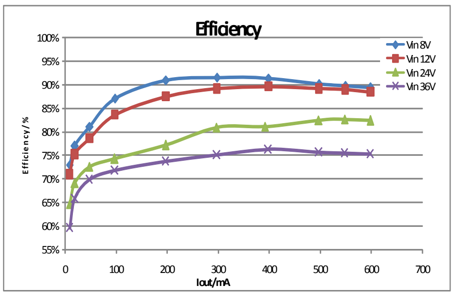
- Distributed Power Systems
- Automotive Systems
- High Voltage Power Conversion
- Industrial Power Systems
- Battery Powered Systems

TYPICAL APPLICATION

5V/600mA Step Down Regulators



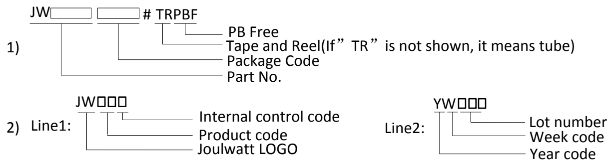
Efficiency @ Vout=5V



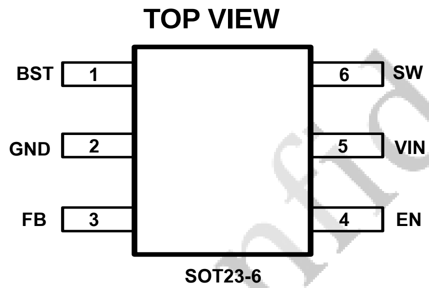
ORDER INFORMATION

DEVICE[1]	PACKAGE	TOP MARKING[2]
JW5018SOTB#TRPBF	SOT23-6	JWHJ□ YW□□□

Notes：



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

VIN, EN, SW Pin .... -0.3V to 44V
BST Pin .... SW-0.3V to SW+5V
All other Pins .... -0.3V to 6V
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature .... -65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN ....4.7V to 40V
Output Voltage Vout..0.8V to VIN-3V
Operating Junction Temperature ....-40ºC to 125ºC

THERMAL PERFORMANCE[4)] θ_{JA} θ_{Jc}

SOT23-6 .... 220...130ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMEND OPERATION CONDITIONS.

2) The JW5018 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25ºC, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
V_{IN} Under voltage Lockout Threshold	V_{IN_MIN}	V_{IN} rising	4	4.3	4.6	V
V_{IN} Under voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			250		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V		0.1	1	μA
Supply Current	I_Q	V_{EN}=5V, V_{FB}=1.2V		40	60	μA
Feedback Voltage	V_{FB}	4.7V<V_{VIN}<40V	776	800	824	mV
Top Switch Resistance[5)]	$R_{DS(ON)T}$			500		mΩ
Bottom Switch Resistance[5)]	$R_{DS(ON)B}$			220		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=40V, V_{EN}=0V, V_{SW}=0V			1	uA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}= V_{SW} = 40V, V_{EN}=0V			1	uA
Top Switch Current Limit[5)]	I_{LIM_TOP}	Minimum Duty Cycle		1		A
Switch Frequency[5)]	f_{SW}			2		MHz
Minimum On Time[5)]	T_{ON_MIN}			80		ns
Minimum Off Time	T_{OFF_MIN}	V_{FB}=0V		100		ns
Maximum On Time	T_{ON_Max}	V_{FB}=0V		3.3		us
EN shut down threshold voltage	V_{EN_TH}	V_{EN} rising, FB=0V	1.18	1.3	1.42	V
EN shut down hysteresis	V_{EN_HYST}			120		mV
Thermal Shutdown[5)]	T_{TSD}			135		°C
Thermal Shutdown hysteresis[5)]	T_{TSD_HYST}			15		°C

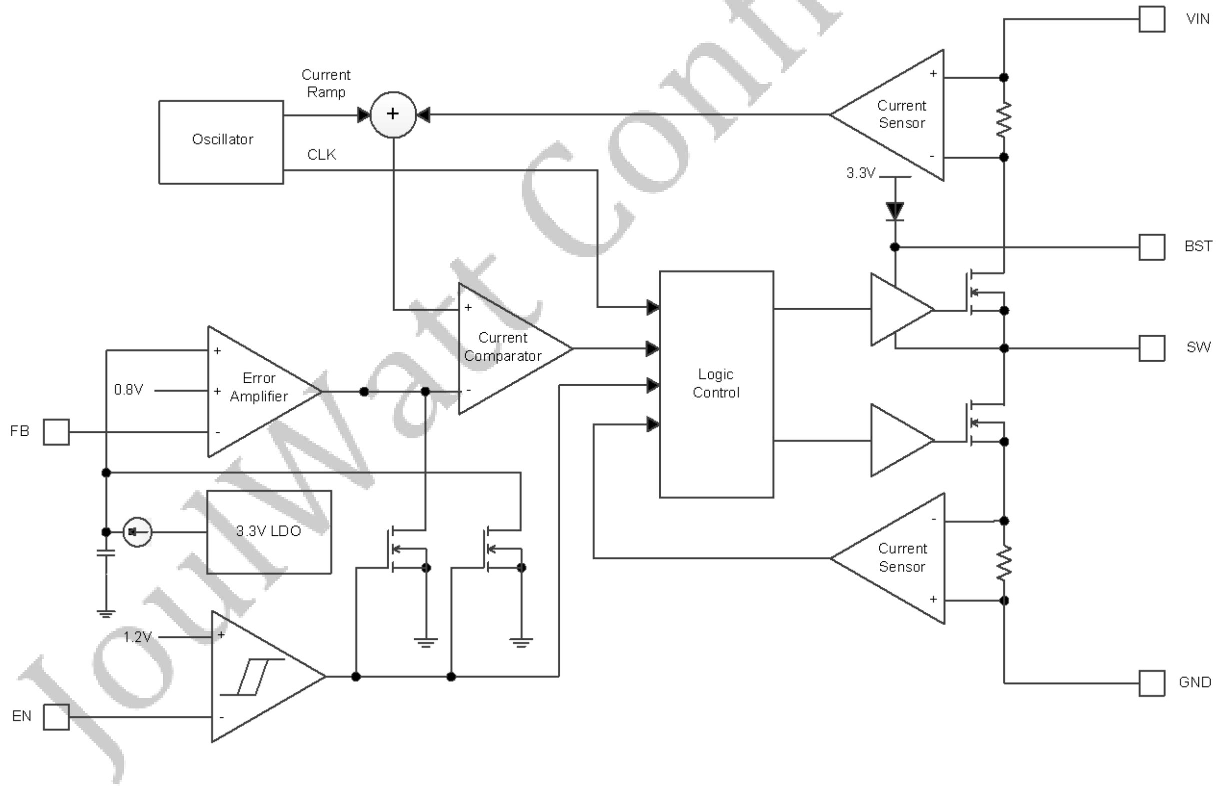
Note：

5) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	BST	Bootstrap pin for top switch.
2	GND	Ground.
3	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 800mV. Connect a resistive divider at FB.
4	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
5	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.7V to 40V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
6	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.

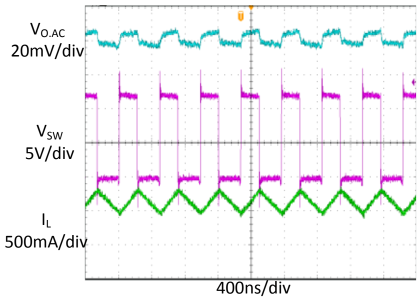
BLOCK DIAGRAM



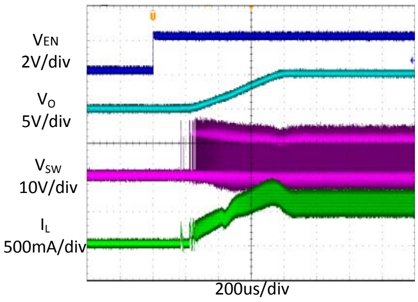
TYPICAL PERFORMANCE CHARACTERISTICS

Vin = 12V, Vout = 5V, L = 4.7μH, Cout = 10μF, TA = +25°C, unless otherwise noted

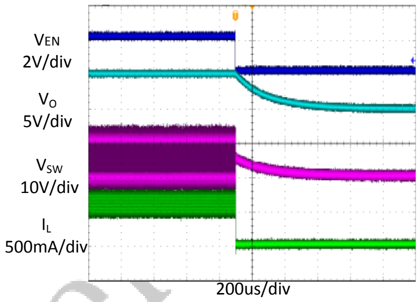
Steady State Test
VIN=12V, Vout=5V
Iout=600mA



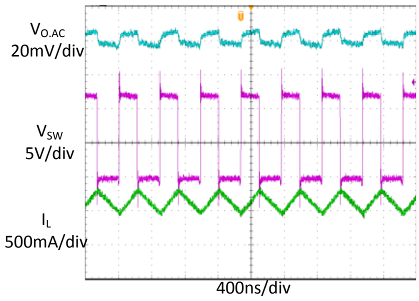
Startup through Enable
VIN=12V, Vout=5V
Iout=600mA(Resistive load)



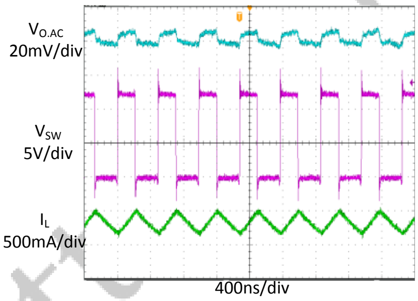
Shutdown through Enable
VIN=12V, Vout=5V
Iout=600mA(Resistive load)



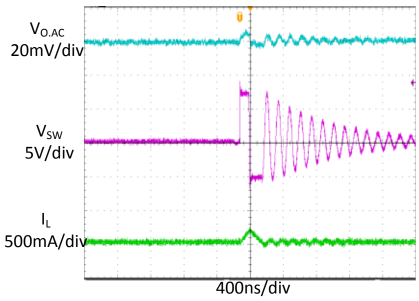
Heavy Load Operation
600mA LOAD



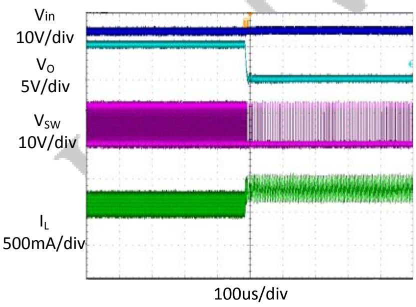
Medium Load Operation
300mA LOAD



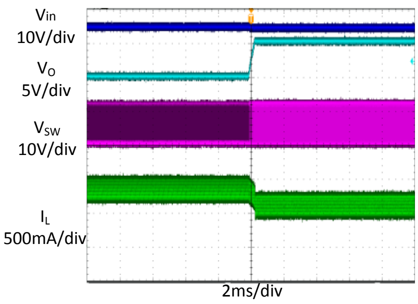
Light Load Operation
0 A LOAD



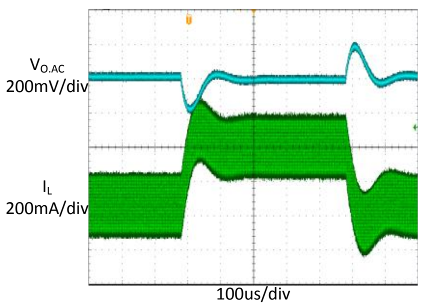
Short Circuit Protection
VIN=12V, Vout=5V
Iout=600mA- Short



Short Circuit Recovery
VIN=12V, Vout=5V
Iout= Short-600mA



Load Transient
300mA LOAD → 600mA LOAD
→ 300mA LOAD

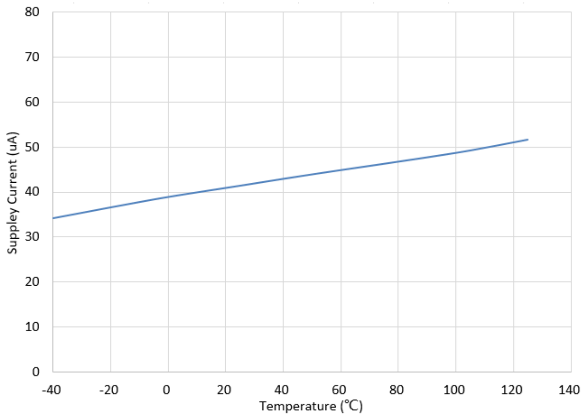


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Vin = 12V, Vout = 5V, L = 4.7μH, Cout = 10μF, TA = +25°C, unless otherwise noted

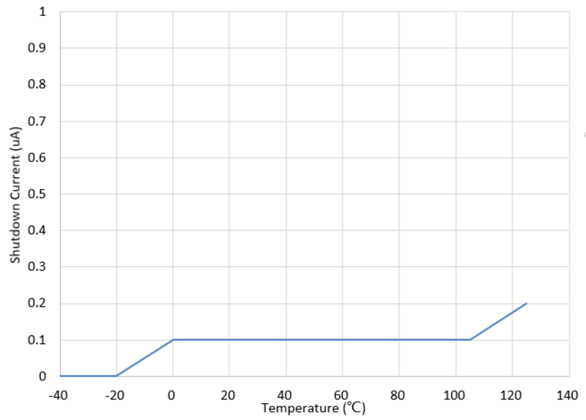
Quiescent Current Vs. Temperature

VIN=12V, VEN=3.3V, VFB=1V



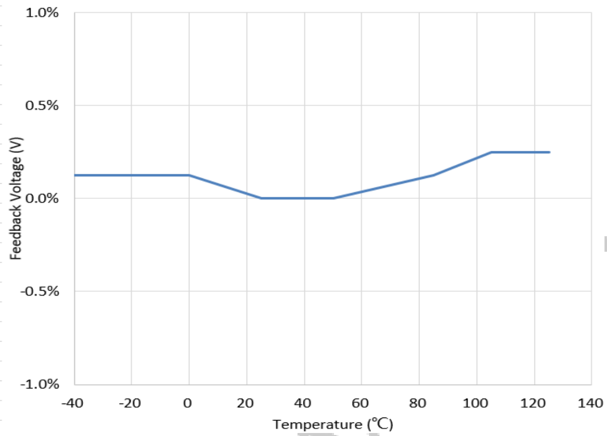
Shutdown Current Vs. Temperature

VIN=12V, VEN=0V, VFB=0.3V



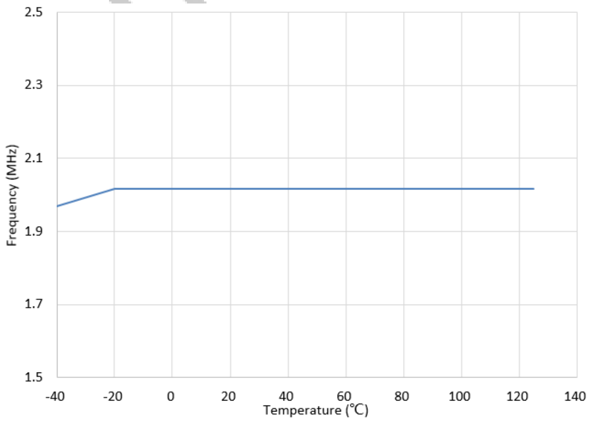
Feedback Voltage Vs. Temperature

VIN=12V, VEN=3.3V



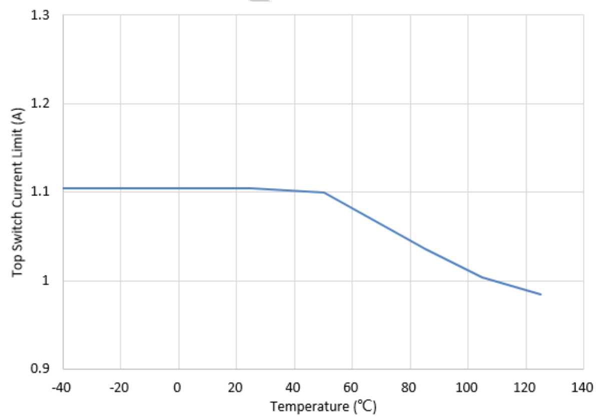
Frequency Vs. Temperature

VIN=12V, VEN=3.3V, Vout=5V, Iout=0.6A



Top Switch Current Limit Vs. Temperature

VIN=12V, VEN=3.3V, Vout Short @ L=4.7uH



FUNCTIONAL DESCRIPTION

The JW5018 is a synchronous, current-mode, step-down regulator. It regulates input voltages from 4.7V to 40V down to an output voltage as low as 0.8V, and is capable of supplying up to 600mA of load current.

Current-Mode Control

The JW5018 utilizes current-mode control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal trans conductance error amplifier.
Output of the internal error amplifier is compared with the switch current measured internally to control the output current.

PFM Mode

The JW5018 operates in PFM mode at light load. In PFM mode, switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

Shut-Down Mode

The JW5018 shuts down when voltage at EN pin is below 0.3V. The entire regulator is off and the supply current consumed by the JW5018 drops below 0.1uA.

Power Switch

N-Channel MOSFET switches are integrated on the JW5018 to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage great than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.3V rail when SW is low.

Low Dropout Operation

The JW5018 is designed to operate at almost 100% duty cycle to improve dropout. When the current in the top switch does not reach the comp-set current value within one PWM cycle, the top switch remains on to prevent a turn-off operation. The top switch can remain on for a maximum of 3.3µs and then turns off for a minimum of 100ns.

Vin Under-Voltage Protection

A resistive divider can be connected between Vin and ground, with the central tap connected to EN, so that when Vin drops to the pre-set value, EN drops below 1.2V to trigger input under voltage lockout protection.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductance can be easily built up, resulting in a large start-up output current. A valley current limit is designed in the JW5018 so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Output Short Protection

When output is shorted to ground, output current rapidly reaches its peak current limit and the top power switch is turned off. Right after the top power switch is turned off, the bottom power switch is turned on and stay on until the output current falls below the valley current limit. When output current is below the valley current limit, the top power switch will be turned on again and if the output short is still present, the top power switch is turned off when the peak current limit is reached and the bottom power switch is turned on. This cycle goes on until the output short is removed and the regulator comes into normal operation again.

Thermal Protection

When the temperature of the JW5018 rises above 135°C, it is forced into thermal shut-down. Only when core temperature drops below 120°C can the regulator becomes active again.

APPLICATION INFORMATION

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_3}{R_2 + R_3}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_3 around 2.1kΩ ~ 5kΩ, and then R_2 can be calculated by:

$$R_2 = R_3 \cdot \left(\frac{V_{OUT}}{0.8V} - 1\right)$$

The following table lists the recommended values.

VOUT(V)	R3(kΩ)	R2(kΩ)
2.5	4.99	11
3.3	4.22	13.3
5	2.1	11.2

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_S \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_1 is the input capacitance value, f_S is the switching frequency, $\triangle V_{IN}$ is the input ripple current.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 4.7uF ceramic capacitor is recommended in typical application, and an extra 47uF electrolytic capacitor is needed if hot-plug is required.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_S \cdot C_2}\right)$$

where C_2 is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 10uF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 30% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_S is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

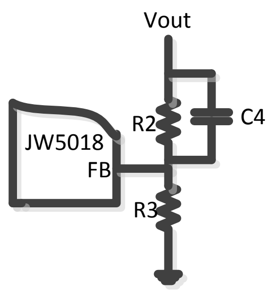
A bootstrap capacitor is required to supply voltage to the top switch driver. A 10nF ~ 0.1uF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

When Duty cycle is higher than 95%, a 10nF bootstrap capacitor is recommended which can enhance the stability of the converter.

(Refer to REFERENCE DESIGN 3 @ page 12)

Feedforward Capacitor

In order to reduce the ripple of Vout at duty cycle is higher than 90%, a feedforward capacitor (C4) is recommended.



PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5018 (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation

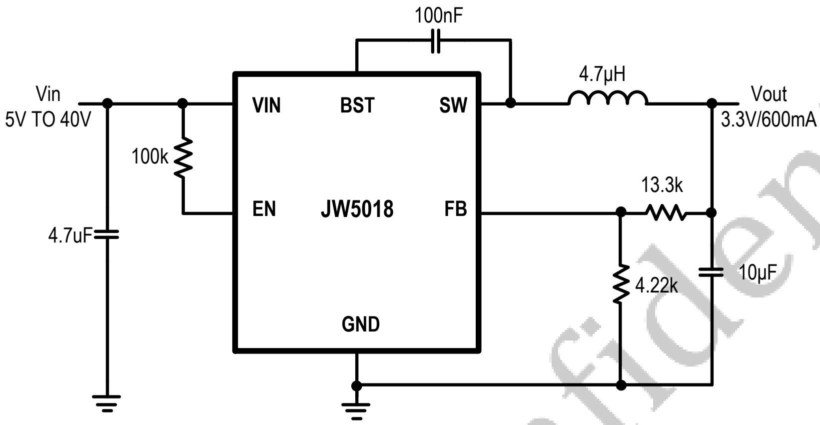
REFERENCE DESIGN

Reference 1:

V_{IN} : 5V ~ 40 V

V_{OUT}: 3.3V

I_{OUT} : 0~600mA

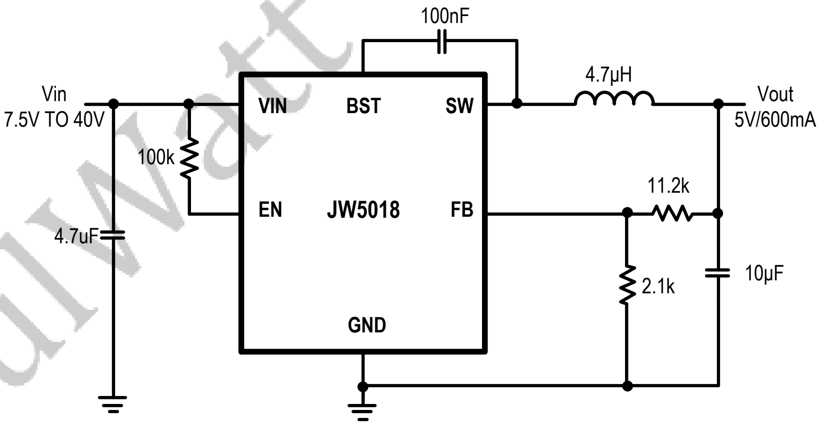


Reference 2:

V_{IN} : 7.5V ~ 40 V

V_{OUT}: 5V

I_{OUT} : 0~600mA



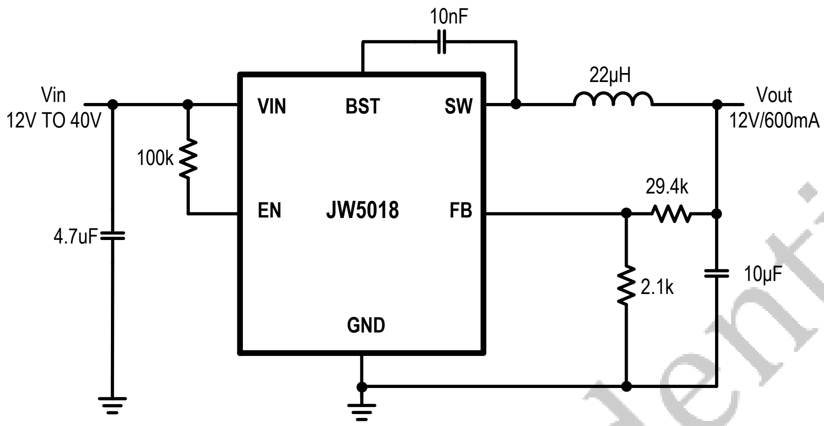
Reference 3：

V_{IN} : 12V ~ 40 V

V_{OUT}: 12V

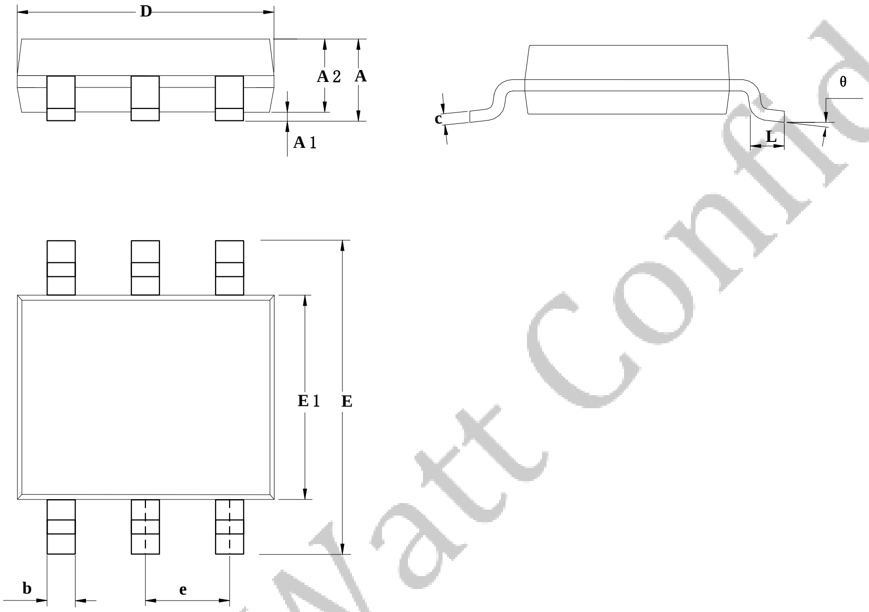
Duty: >= 95%

I_{OUT} : 0~600mA



PACKAGE OUTLINE

SOT23-6 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	1.15	1.25
A1	0	0.05	0.15
A2	0.95	1.10	1.20
b	0.20	0.40	0.60
c	0.05	—	0.21
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95（BSC)		
L	0.30	0.45	0.60
θ	0°	—	8°

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