Features

- High Efficiency up to 96%
- I2C interface
- Dynamic adjustable output voltage Support PD3.0 (PPS) and QC4.0
- Dynamic adjustable input and output current limit
- 2.7V to 36V Input Voltage Range
- 2.0V to 36V Output Voltage Range
- adjustable VCC voltage
- integrated BST diode
- adjustable frequency200kHz 400KHz 600KHz
- Short Circuit Protection
- Thermal Fault Protection
- Inrush Current Limit and Soft Start
- Under voltage protection
- QFN32L-4×4 package

Applications

- Car charger
- USB PD device
- Power bank

General Description

The SP1260HN is a synchronous 4-switch buck-boost controller. It is able to effectively output voltage no matter it is higher, lower or equal to the input voltage.

The SP1260HN supports very wide input and output voltage range. It can support applications from 2.7V to 36V input range and 2V to 36V output range. The driver voltage is can be set to 5V、7.5V or 10V to various external MOSFETs for best efficiency.

The SP1260HN supports input current limit, output current limit and over temperature protections to ensure safety under different abnormal conditions.

The SP1260HN adjustable output voltage input current limit output current limit used I2C interface.

Simplified Application

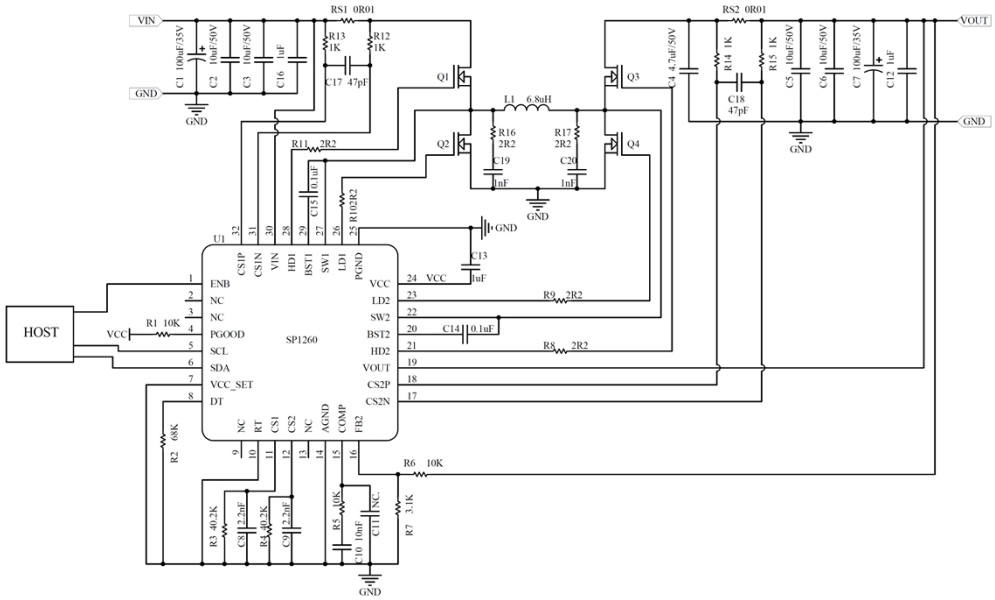


Figure 1.Simplified Application of SP1260HN

Pin Function Description

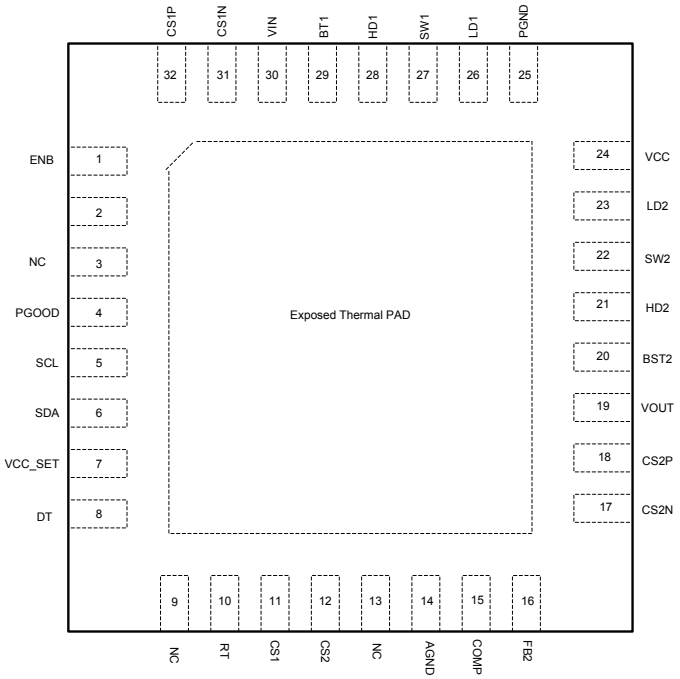


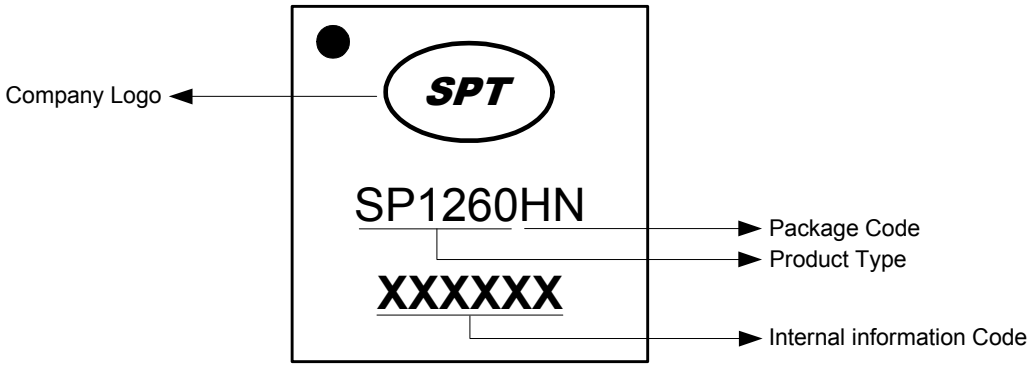
Figure 2.Top View

Pin No.	Pin Name	Function Description
1	ENB	Chip Logic Enable ENB=low chip enable. Internal pull low.
2	NC	
3	NC	
4	PGOOD	Open drain, active high when VOUT is within 90% to 110% * VOUT target.
5	SCL	I2C BUS clock signal. Not floating
6	SDA	I2C BUS data signal. Not floating
7	VCC_SET	VCC output voltage selection. Short to ground: 5V; 68kΩ: 7.5V; Open: 10V
8	DT	Dead time selection. Short to ground: 20ns; 68kΩ: 40ns; 270kΩ: 60ns; Open:80ns.
9	NC	
10	RT	Frequency selection. Short to ground: 200kHz; 68kΩ: 400kHz; Open: 600kHz.
11	CS1	Connect a resistor to set the current limit value of input current. A 2.2nF capacitor to ground is needed to bypass noise.
12	CS2	Connect a resistor to set the current limit value of output current. A 2.2nF capacitor to ground is needed to bypass noise.
13	NC	

14	AGND	Analog GND
15	COMP	Internal error amplifier output pin .Connect a capacitor and a resister in series to AGND for loop compensation
16	FB	VOUT voltage feedback pin .Connect a resister divider from VOUT to FB.
17	CS2N	Negative input of current sense amplifier. Connect an external current sense resistor between CS2P and CS2N. Current flows from CS2P to CS2N.
18	CS2P	Positive input of current sense amplifier. Connect an external current sense resistor between CS2P and CS2N. Current flows from CS2P to CS2N.
19	VOUT	V_{OUT} voltage sense input. It also supplies power to VCC base on VCC power logic. Connect a 1uF capacitor to GND near by the IC.
20	BST2	Bootstrap power pin for boost high side MOSFET gate driver. Connect a capacitor between BST2 and SW2.It is supplies VCC or BST1.
21	HD2	Boost high-side MOSFET gate driver pin.
22	SW2	Boost switch node of converter.
23	LD2	Boost low-side MOSFET gate driver pin.
24	VCC	Driver circuit bias supply. Decouple with a 1uF or more ceramic capacitor as close to this pin as possible. It is power by VIN or VOUT.
25	PGND	Power ground
26	LD1	Buck low-side gate driver.
27	SW1	Buck switch node of converter.
28	HD1	Buck high-side MOSFET gate driver pin.
29	BST1	Bootstrap power pin for buck high side MOSFET gate driver. Connect a capacitor between BST1 and SW1.It is supplies VCC or BST2.
30	VIN	VIN power supply and voltage input. Decouple with a 1uF or more ceramic capacitor as close to this pin as possible
31	CS1N	Negative input of current sense amplifier. Connect an external current sense resistor between CS1P and CS1N. Current flows from CS1P to CS1N.
32	CS1P	Positive input of current sense amplifier. Connect an external current sense resistor between CS1P and CS1N. Current flows from CS1P to CS1N.
33	Thermal PAD	Thermal PAD

Ordering and Marking Information

Part Number	Package Description	Top Marking	Package Form
SP1260HN	QFN32L-4X4	SP1260HN	QFN32L-4X4



Absolute Maximum Ratings

Characteristics	Symbol	Rating	Units
Supply Input Voltage	V_{IN}	-0.3 to +42	V
Output Voltage	V_{OUT}	-0.3 to +42	V
SW1 SW2	V_{SW}	-0.3 to +42	V
CS1P CS1N CS2P CS2N ENB		-0.3 to +42	V
BT1 HD1 to SW1		-0.3 to +12	V
BT2 HD2 to SW2		-0.3 to +12	V
LD1 LD2		-0.3 to +12	V
VCC PG		-0.3 to +20	V
SCL SDA DT COMP CS1 CS2 RT VCC_set FB		-0.3 to +5.5	V
ESD HBM(Human Body Mode)		±2K	V
ESD MM(Machine Mode)		±200	V
Power Dissipation, PD @T_A=25℃	P_D	$(T_J-T_A)/\theta_{JA}$	W
Thermal Resistance from Junction to case	θ_{JC}	tdb	℃/W
Thermal Resistance from Junction to ambient	θ_{JA}	tdb	℃/W

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Description	Value	Units
V_{IN}	Input Voltage Range	2.7 ~ 36.0	V
V_{OUT}	Output Voltage Range	2.0 ~ 36.0	V
C_{IN}	Minim Input Capacitance	30	uF
C_{OUT}	Minim Input Capacitance	30	uF
L	Inductance	2.2 ~ 10.0	uH
Rcs1/2	Current Sensing Resistor	5.0 ~ 20.0	mΩ
f_{SW}	Operating frequency range	200~600	kHz
T_{ST}	Storage Temperature Range	-65 to +150	℃
T_J	Junction Temperature	-40 to +125	℃
T_{OP}	Operating Temperature	-40 to +85	℃
	Lead Temperature Range(Soldering 10sec)	260	℃

Note:

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A= 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Block Diagram

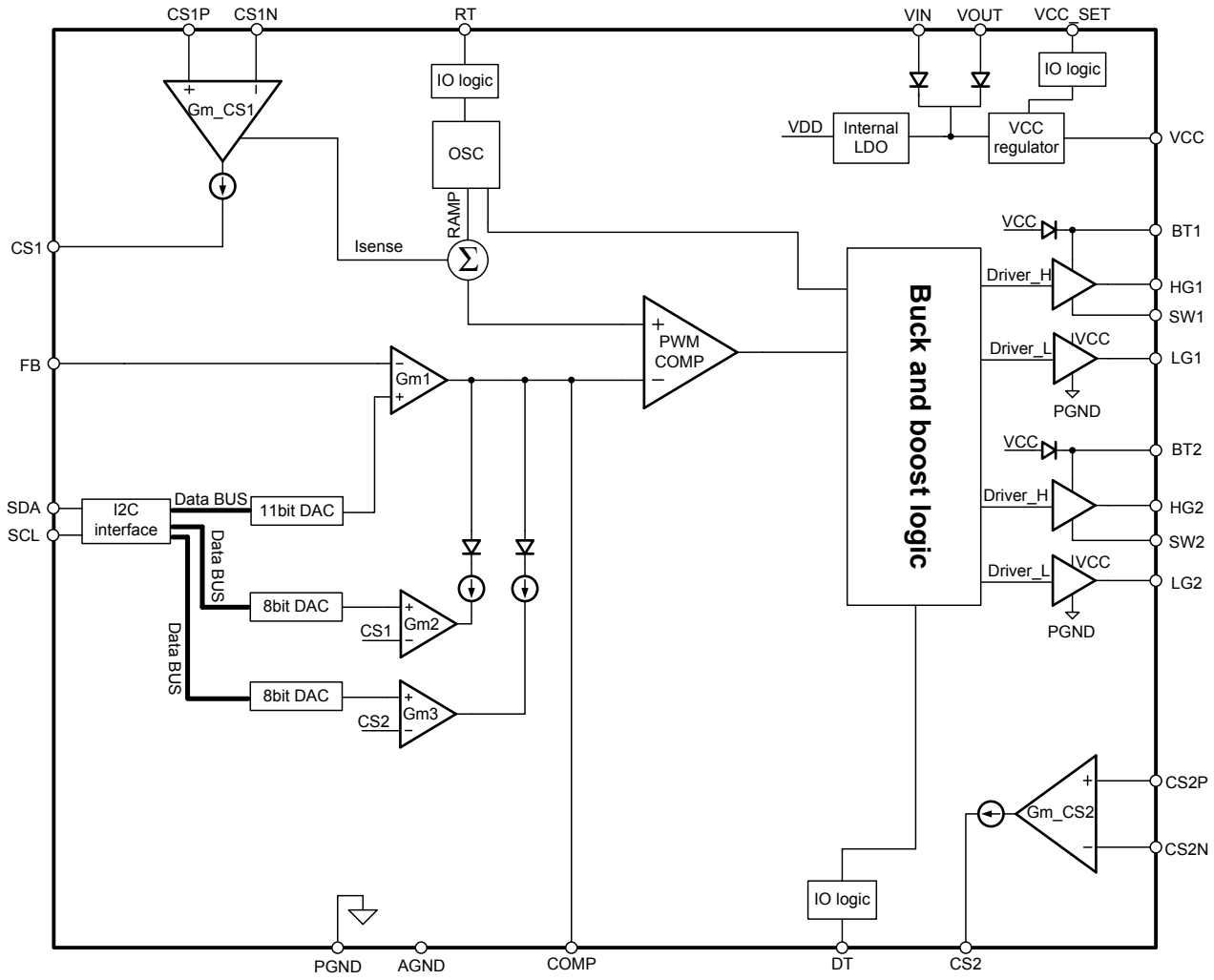


Figure 3.Block diagram of SP1260HN

Electrical Characteristics

(V_{IN} =12V, V_{OUT}=5V, T_A =+25°C, unless otherwise specified)

symbol	Parameter	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN	Input voltage range		2.7		36	V
VOUT	Output voltage range		2		36	V
V_{UVLO}	Input under voltage lockout threshold	Rising edge		2.6	2.7	V
		Hysteresis		0.16		V
I_{CC}	standby current Into VIN or VOUT pin (which is higher)	ENB=low, controller no-switching		0.7	2	mA
I_{SD}	Shutdown current Into VIN or VOUT pin (which is higher)	ENB=high		6	10	uA
	Shutdown current Into VIN or VOUT pin (which is lower)	ENB=high			2	uA
VCC AND DRIVER						
V_{CC}	VCC output voltage	Rvcc_set =0Ω		10		V
		Rvcc_set =68kΩ(±10%)		7.5		V
		Rvcc_set =270kΩ(±10%)		5.0		V
I_{VCC_LIM}	VCC current limit		50	75	100	mA
R_{HD}	HD1 HD2 Pull up Resistance			1.5		Ω
R_{LD}	LD1 LD2 Pull down Resistance			1.0		Ω
TD	Dead time	RDT=0Ω		20		ns
		RDT=68kΩ(±10%)		40		ns
		RDT=270kΩ(±10%)		60		ns
		RDT=floating		80		ns
ERROR AMPLIFIER						
Gm_{EA}	Error Amplifier gm			160		uS
R_{OUT}	Error Amplifier output resistance			20		MΩ
I_{FB}	FB pin input current				100	nA
VREF						
V_{REF_EA}	DAC output reference voltage	VREF[bit10:0]=00111110100	495	500	505	mV
		VREF[bit10:0]=10010110000	1194	1200	1206	
		VREF[bit10:0]=11111010000	1990	2000	2010	
V_{REF_CL}	DAC output reference voltage for current limit of input	ILIMx[bit7:0]=11111111		1.201		V
		ILIMx[bit7:0]=10000000		0.6		V
Switching Frequency						
f_{SW}	Switching Frequency	RRT=0Ω		200		kHz
		RRT =68kΩ(±10%)		400		kHz
		RRT =270kΩ(±10%)		600		kHz

INDICATION						
tPG_deglitch	PG signal deglitch time	FSW=200kHz	27	38.5	50	ms
Isink_PG	PG sink current	VPG=0.4V	3.6	4.1	4.6	mA
Vout_PG				110%		
				5%		
				90%		
				5%		
LOGIC INPUT						
Rpulldown	ENB pull down resistor			1		MΩ
VIL	ENB,SDA,SCL input low voltage				0.4	V
VIH	ENB,SDA,SCL input low voltage		1.2			V
RSDA	SDA open drain resistance			50		Ω
THERMAL SHUTDOWN						
TSD	Thermal shutdown temperature			165		℃
	Thermal shutdown Hysteresis			30		℃

Functional Description

The SP1260HN is a synchronous four-switch buck-boost controller with a wide input/output voltage range. The SP1260HN regulates the output at, above, below the input voltage. The SP1260HN features automatic buck, boost mode smooth transition and maximum input and output current limit capability using additional resistors. In addition, the SP1260HN features output voltage dynamic change, input/output current limit dynamic change, and power MOSFETs dead time control.

Chip Enable (ENB)

The SP1260HN turns on/off by ENB signal. When ENB input is “L”, the SP1260HN is turned on; when ENB input is “H”, The SP1260HN is turned off.

Output voltage setting (FB)

The VOUT voltage is set by external resistor divider at FB pin and is calculated as:

$$VOUT = VREF \times (1 + \frac{R_{UP}}{R_{DOWN}})$$

$$VREF = 2048mV \times \frac{VREF[bit10:0]}{2048}$$

Where the VREF[bit10:0] is the data write in REG01 and REG02.RUP and RDWON Resistor divider at FB connected to VOUT and AGND.

Output voltage POWER GOOD indicator (PG)

The PG signal indicates VOUT voltage status. If VOUT voltage remains in between 90% ~ 110% of programmed voltage, PG pin becomes high impedance and due to the output pull-up resistor, PG out becomes “H” to indicate the output voltage is good. If VOUT is out of normal voltage range, PG out becomes “L”. If power good indication is not required, leave PG pin floating.

Input/output current setting (CSx)

The SP1260HN can adjust the current limit of both input side and output side by resistors at CS1 and CS2 pins. The current limit is set by external resistor and is calculated as:

$$I_{LIMIT\_IN} = 1.22V \times \frac{ILIM1[bit7:0]}{255} \times \frac{R_{CS1P}}{R_{CS1} \times R_{sense1}}$$

$$I_{LIMIT\_OUT} = 1.22V \times \frac{ILIM2[bit7:0]}{255} \times \frac{R_{CS2P}}{R_{CS2} \times R_{sense2}}$$

ILIMI1[bit7:0] and ILIMI2[bit7:0] is the data write in the REG03H and REG04H.RCSx is the resistor from CSx to ground. Rsensex is current sensing resistor. Recommended 5mΩ-20mΩ，typical 10mΩ； RCSxP are the resistors connected to CSxP， CSxN. The two resistors must be equal and the recommended value is 1kΩ. A 2.2nF capacitor to ground is needed to bypass noise. If IPWM function is applied to ILIM2, increase the capacitor value to 10nF. If current limiting function is not needed, please short ILIM2 to ground.

I2C interface

The SP1260HN uses I2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I2C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial dataline (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address D6h, receiving control inputs from the master device like micro controller or a digital signal processor through REG01-REG07. The I2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). Connect to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

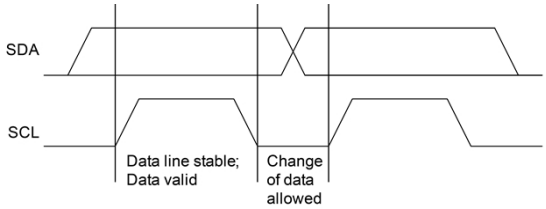


Figure 4. Bit Transfer on the I2C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

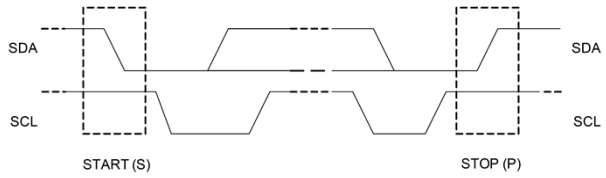


Figure 5. START and STOP condition

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is Unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

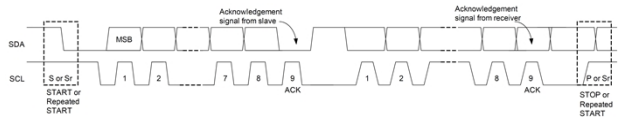


Figure 6. Data Transfer on the I2C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse. When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

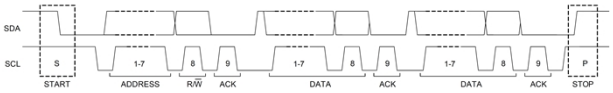


Figure 7. Complete Data Transfer

Single Read and Write

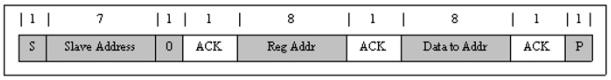


Figure 8. Single Write

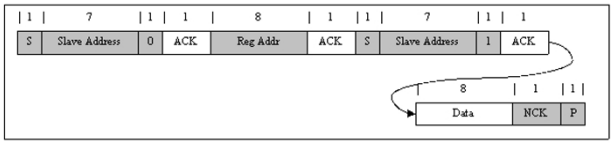


Figure 9. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

Multi-Read and Multi-Write

The charger device supports multi-read and multi-write.

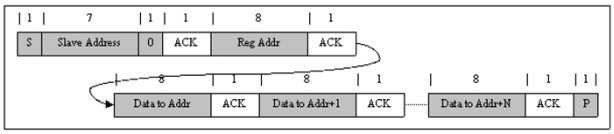


Figure 10. Multi Write

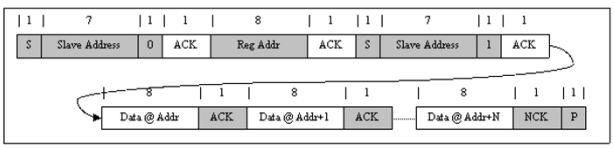


Figure 11. Multi Read

Register Map

Device address =74H											
Addr	**Register**	**Type**	**Default Value**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
01H	REF_MSB	R/W	00111110	VREF[bit10:3]							
02H	REF_LSB	R/W	100xxxxx	VREF [bit2:0]			reverse				
03H	ILIM1	R/W	11111111	ILIM1 [bit7:0]							
04H	ILIM2	R/W	11111111	ILIM2 [bit7:0]							
05H	REF2	R/W	11111111	reverse							
06H	Control1	R/W	00000000	SR[1:0]			reverse				
07H	Control2	R/W	00000000	reverse							

Register Name: REF_MSB , Read/Write

Name	Bits	Default Value	Description
VREF[bit10:3]	D[10:3]	01111110	Feedback voltage reference VREF high 8 bit .LSB=8mV. Total 11bit set VREF from 0mV to 2047mV

Register Name: REF_LSB , Read/Write

Name	Bits	Default Value	Description
VREF [bit2:0]	D[2:0]	100	Feedback voltage reference VREF low 3 bit .LSB=1mV. Total 11bit set VREF from 0mV to 2047mV

Register Name: ILIM1, Read/Write

Name	Bits	Default Value	Description
ILIM1 [bit7:0]	D[7:0]	11111111	Input current limit voltage reference LSB=4.8mV. Total 8bit set $VREF_{ILIM1}$ from 0mV to 1220mV

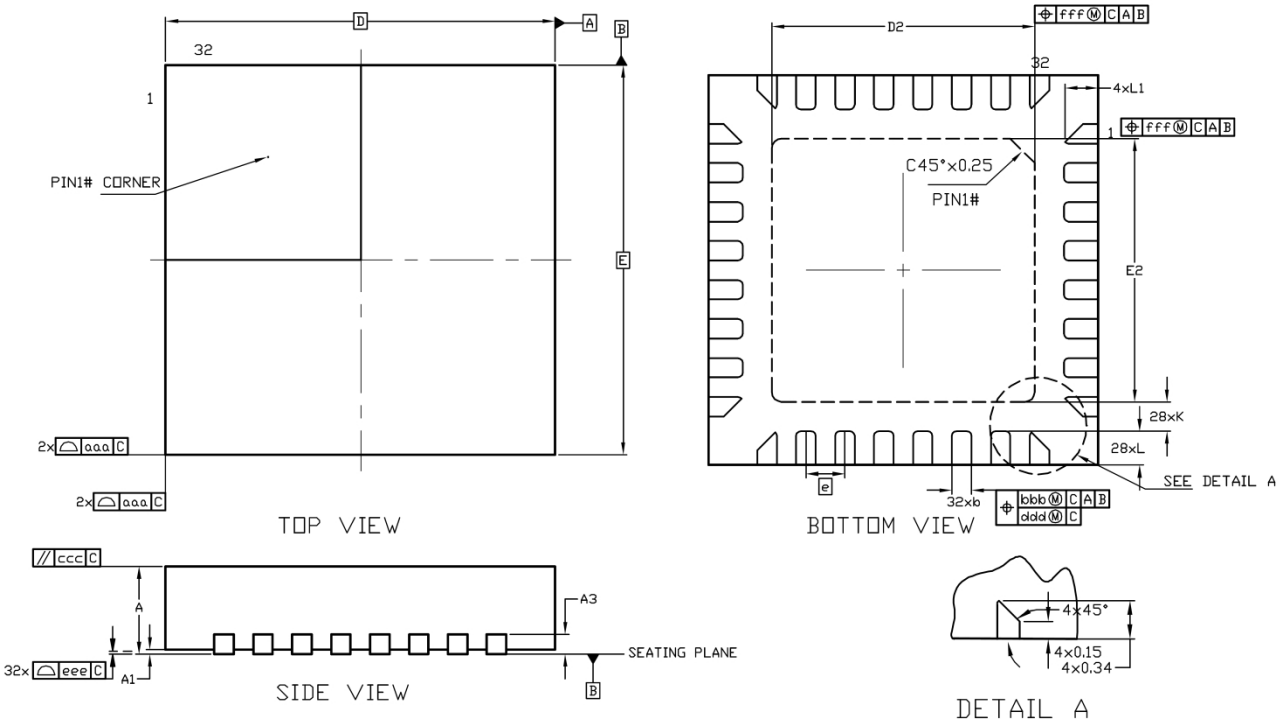
Register Name: ILIM2, Read/Write

Name	Bits	Default Value	Description
ILIM2 [bit7:0]	D[7:0]	11111111	Output current limit voltage reference LSB=4.8mV. Total 8bit set $VREF_{ILIM2}$ from 0mV to 1220mV

Register Name: control1, Read/Write

Name	Bits	Default Value	Description	
SR [bit1:0]	D[1:0]	00	The VREF slew rate set.	
			SR bit value	VREF slew rate
			00	0.45mV/us
			01	0.9mV/us
			10	1.8mV/us
			11	3.6mV/us

Package Information（Units:mm）



Symbol	Dimensions in Millimeters		
	Min.	TYP.	Max.
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3	-	0.152 REF	-
b	0.15	0.20	0.25
D	4.00BSC		
E	4.00BSC		
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e	0.40BSC		
L	0.35	0.40	0.45
K	0.25 REF		
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

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