

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JW7726HAE is a synchronous rectifier, used for the secondary side rectification of isolation topologies, such as Active Clamp Flyback and CCM/QR/DCM Flyback. JW7726HAE is able to significantly improve the efficiency comparing with the conventional Diode rectifier.

When JW7726HAE senses V_{ds} of MOSFET less than $-140mV$, it turns on the internal MOSFET. Once the V_{ds} is greater than $-6mV$, JW7726HAE turns off the internal MOSFET.

JW7726HAE supports multiple operation modes, such as DCM, CrCM, CCM and Quasi-Resonant. By implementing the Joulwatt proprietary technology, JW7726HAE is able to handle CCM operation.

JW7726HAE is available in PVDFN5*6-8 package.

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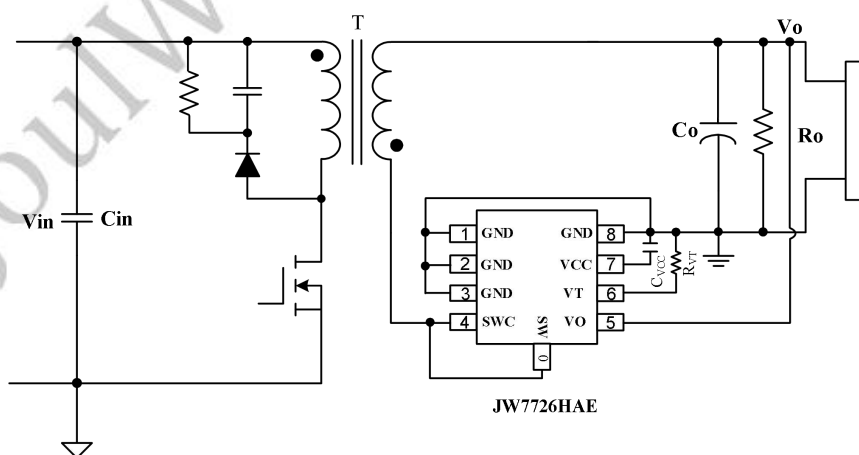
FEATURES

- Supports Active Clamp Flyback, DCM, Quasi-Resonant, and CCM Flyback
- Support High-side and Low-side Rectification
- Output Voltage Directly Supply VCC
- Low Quiescent Current
- Fast Driver Capability for CCM Operation
- PVDFN5*6-8 Package

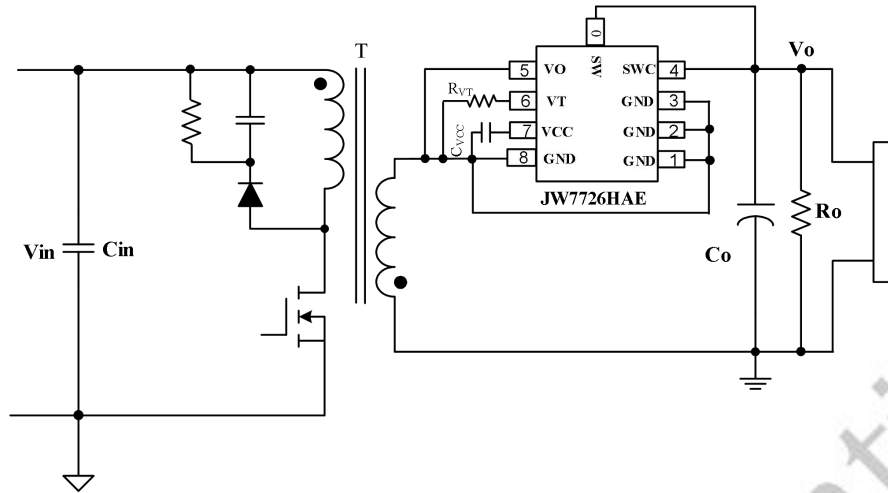
APPLICATIONS

- Active Clamp Flyback and Flyback Converters
- Adaptor
- LCD and PDP TV

TYPICAL APPLICATION



JW7726HAE Typical Application for Low-side



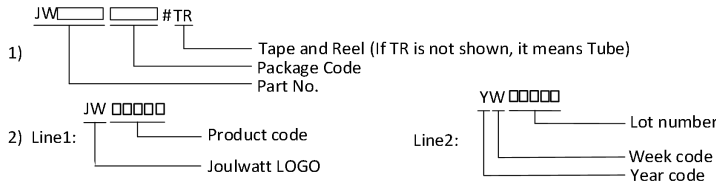
JW7726HAE Typical Application for High-side.

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ORDER INFORMATION

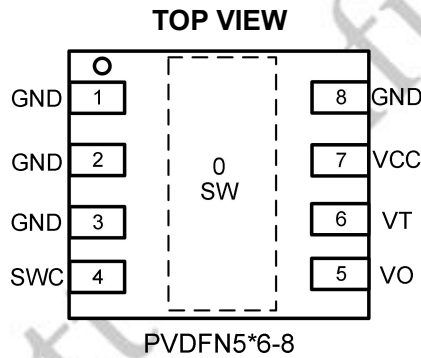
DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾	ENVIRONMENTAL ³⁾
JW7726HAEPVDLQF#TR	PVDFN5*6-8	JW7726HAE YW□□□□□	Green

Notes :



3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING¹⁾

SW PIN	100V
SWC PIN	-1 to 100V
VO PIN	-0.3 to 28V
VCC PIN.....	-0.3 to 9V
VT PIN.....	-0.3 to 7V
Junction Temperature ^{2) 3)}	150°C
Lead Temperature	260°C
Storage Temperature.....	-65°C to 150°C
Continuous Power Dissipation(T _A =+25°C) ⁴⁾ ESOP-8.....	2.5W
ESD Susceptibility (Human Body Model)	2kV

RECOMMENDED OPERATING CONDITIONS

SW Pin.....	4.7V to 80V
SWC Pin.....	4.7V to 80V
VO Pin.....	4.7V to 25V
VCC PIN.....	4V to 8.5V
Operation Junction Temperature(T _J).....	-40°C to 125°C

THERMAL PERFORMANCE⁵⁾

	θ_{JA}	θ_{JC}
PVDFN5*6-8.....	50.....	3°C/W

Note:

- 1) Exceeding these ratings may damage the device. These stress rating do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
- 2) Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$.
- 5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

TA = 25°C, unless otherwise stated

Advance Information, not production data, subject to change without notice.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
<i>VCC Section</i>						
VCC Voltage	VCC	SW=40V, VCC=2.2uF	7.4	7.9	8.4	V
VCC Startup Voltage	V _{CC_Startup}		4.2	4.5	4.8	V
VCC UVLO	V _{CC_UVLO}		3.7	3.95	4.2	V
Operation Current (GT On)	I _{VCC}	GT=5nF, VCC=2.2uF	0.7	0.9	1.1	mA
Quiescent Current	I _q	VCC=4.5V, VCC=2.2uF	100	120	140	uA
<i>SWC and VO Section</i>						
Internal MOS Turn on Threshold	V _{MOS_ON}		-170	-140	-110	mV
Internal MOS Turn off Threshold ⁶⁾	V _{MOS_OFF}			-6		mV
Internal MOS Minimum on Time ⁶⁾	T _{MIN_ON}			560		ns
Turn-on Total Delay ⁶⁾	T _{DON}			50		nS
Turn-off Total Delay ⁶⁾	T _{DOF}			20		nS
VCC Charge Current	I _{SW_CHG}	SW=40V, VCC=6V	75	95		mA
VO Enable Charge Voltage	V _{O_EN}	VCC=4V, SW=0V, rising	4.48	4.6	4.8	V
VO Disable Charge Voltage	V _{O_DIS}	VCC=4V, SW=0V, falling	4.4	4.55	4.7	V
VO Charge Current	I _{VO_CHG}	SW=0V, VCC=6V, VO=12V	28	40	52	mA
<i>Internal MOSFET(SW) Section</i>						
Internal MOSFET Rdson	Rdson	VGT=10V		5.8		mΩ
Breakdown Voltage	B _{(BR)DSS}		100			V

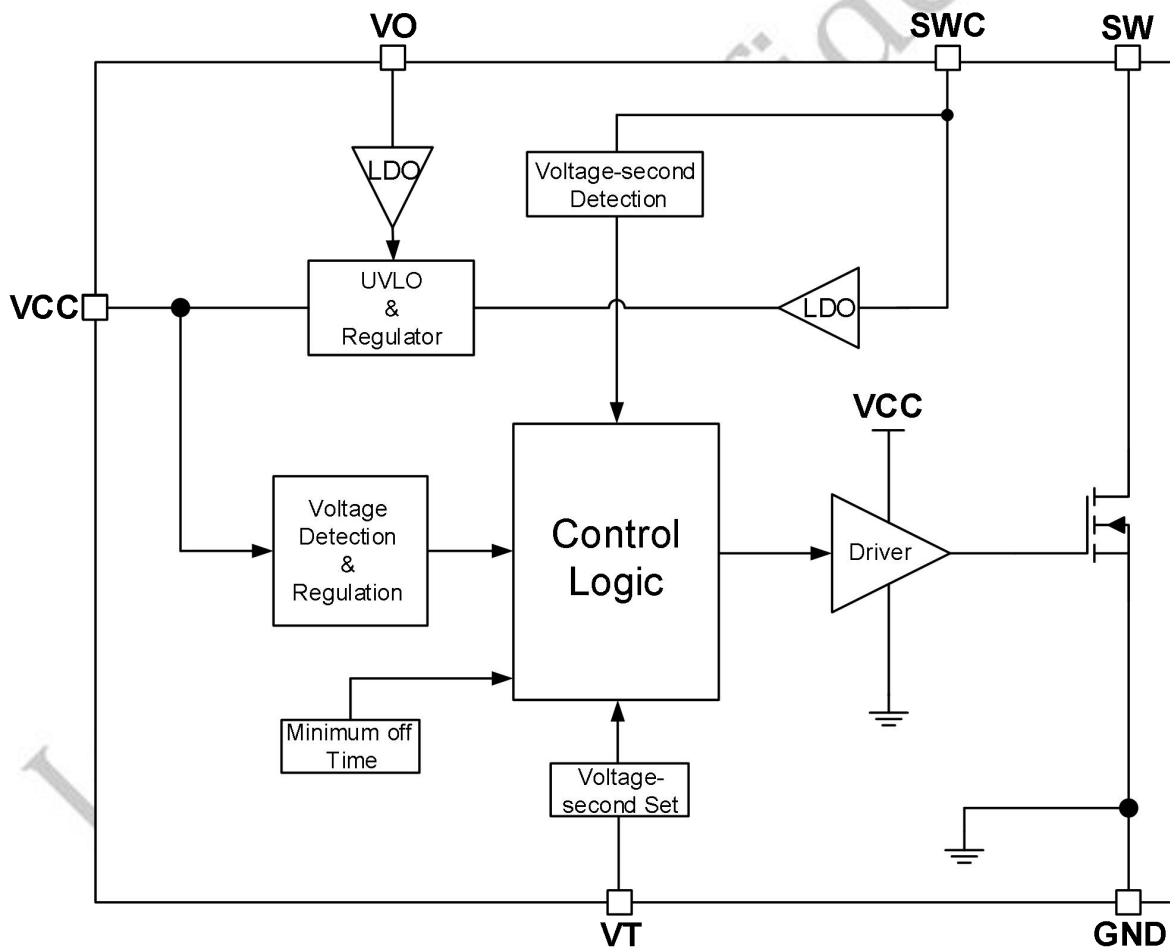
Note:

6) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1,2,3,8	GND	Ground.
4	SWC	Internal Power MOSFET Drain Voltage Sensing. Charging to VCC.
5	VO	Output Voltage Sensing and Charging to VCC.
6	VT	Set the Voltage-second Product.
7	VCC	Power Supply. Bypass a Capacitor Between VCC and GND.
0	SW	Internal Power MOSFET Drain.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Operation

JW7726HAE is a synchronous rectifier controller which combined with external MOSFET can replace the Schottky Barrier Diode. It supports all operations, such as DCM, CrCM, (Quasi-Resonant) and CCM when adopted in Active Clamp Flyback and Flyback converters.

Startup

During the startup period, when the VCC is charged up by the two internal LDOs connected to SW and VO pin respectively.

When VO is lower than 4.55V (falling), JW7726HAE can power itself through the internal LDO connected to SW pin during the SR turn-off period, which means primary the primary side MOSFET is turned on and SW presents a positive voltage. A capacitor between VCC and GND is required to store the energy and supply to IC during the SR turn-on period.

When VO is above 4.65V (rising), the VO pin charges VCC pin.

Once the VCC voltage exceeds $V_{CC_Startup}$, the JW7726HAE exits the UVLO. If VCC is lower than V_{CC_UVLO} , the external MOSFET is turned off. The current flows though body diode before the VCC reaches to the startup voltage $V_{cc_startup}$.

Under-Voltage Lockout (UVLO)

When the VCC is below UVLO threshold, the external MOSFET is turned off and pulled low internally. Once the VCC exceeds the startup voltage $V_{cc_startup}$, the parts is activated again.

Turn On Phase

There are two conditions for the JW7726HAE to turn on the SR, i.e. V_{sw} , voltage-second value on SW pin when primary side switch is on, and the turn on phase is shown in Fig. 1.

1) V_{sw} : when the synchronous MOEFET is conducting, current flows through the body diode of MOSFET, which generates a negative voltage V_{SW} across it. When V_{SW} is lower than V_{MOS_ON} , the part will pull the gate high to turn on the synchronous MOSFET after turn on delay time T_{DON} if the other condition is met.

2) Volt-second of SW: in DCM and QR operation, there are parasitic oscillations. In some applications, the drain resonant voltage may fall below the SR turn on threshold, especially for the first couple rings. SR could be falsely turned on, which may cause shoot through issue and result in high power loss. The volt-second value of SW pin can be used to distinguish the parasitic ring from normal primary side switch on. The threshold can be set by the resistance at VT pin. The curve is shown in Fig. 2.

In application, as the output load(I_o) of converter increases, the volt-second value($S1$) of SW pin also increases. When the volt-second value($S1$) of SW pin is greater than the high threshold and gate turns on, the high threshold becomes to low threshold. As the output load decreasing, when the gate turns off and the MOSFET bodydiode conduction time is no shorter than $T_{on_min.}$, the low threshold becomes to the high threshold. When the R_{vt} is more than $250k\ \Omega$, the high threshold is fixed and the low threshold increases with the increasing of R_{vt} . The low threshold is fixed and equal to the high threshold when the R_{vt} is more

than 330k Ω . The voltage-second hysteresis is shown in Fig. 2 and Fig. 3.

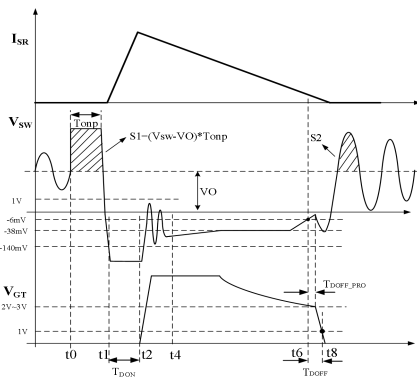


Fig. 1 Turn on delay and turn off delay

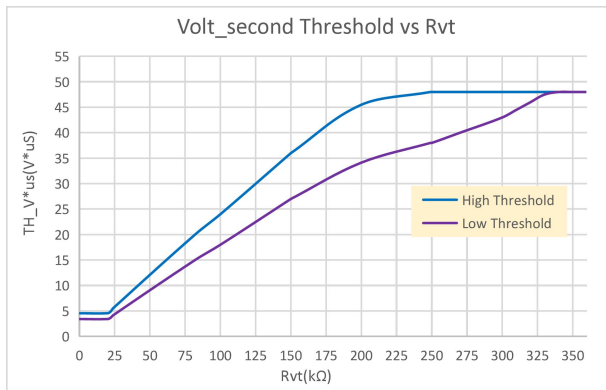


Fig. 2 Volt-second value vs. VT resistance

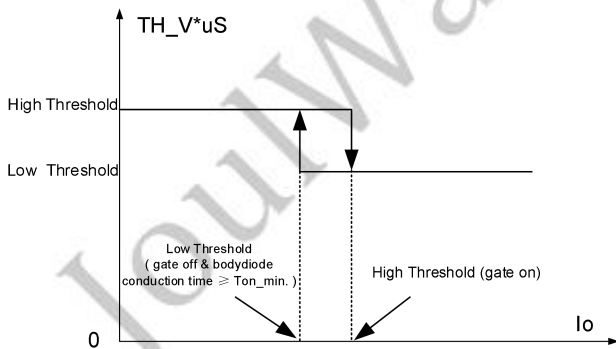


Fig. 3 Volt-second value with hysteresis

Minimum On Time (MOT)

When the synchronous MOSFET is turn on, there is a minimum on time for the SR. The Vsw voltage may have a parasitic ring when the

synchronous MOSFET turns on. So, a minimum on time (MOT) is very important to avoid the MOSFET turn off threshold is false triggered.

Minimum on time is 510ns for high frequency applications.

Conducting Phase

When the synchronous MOSFET is turned on, the drain source voltage Vsw it is determined by its on resistance and the current through it. The part adjusts the gate voltage and regulates the Vsw to the internal threshold (typical -38mV) after the synchronous MOSFET turn on. When the Vsw is lower than -38mV, the gate keeps its maximum voltage. And the synchronous MOSFET is fully on.

The Vsw rises when the current follow through the MOSFET decreases. The gate voltage will be decreased to increase its on resistance and regulate the Vsw around -38mV.

It should be noted that the typical regulation threshold (-38mV) during MOSFET on time is not fixed, it can be internally changed to ensure the proper operation under CCM mode.

Turn Off Phase

After synchronous MOSFET conducting, once the voltage VSW touches the MOSFET turn off threshold (-6mV), the gate is pulled to low after a turn off delay time TDOFF. A 330nS blanking time is necessary to avoid error trigger. The banking time is reset once Vsw rises above 2.5V.

Output Voltage Detection

The JW7726HAE has output voltage detection function via VO pin. VCC is charged from VO pin when VO is higher than 4.65V to save power loss caused by the LDO when charging from SW pin to VCC pin. When VO drops below

4.55V, the JW7726HAE is powered from SW pin.

The V_{SW} rises when the current follow through the MOSFET decreases. The gate voltage will be decreased to increase its on resistance and regulate the V_{SW} around -40mV.

It should be noted that the typical regulation threshold (-40mV) during MOSFET on time is not fixed, it can be internally changed to ensure the proper operation under CCM mode.

Turn Off Phase

After synchronous MOSFET conducting, once the voltage V_{SW} touches the MOSFET turn off threshold , the gate is pulled to low after a turn off delay time T_{DOFF} .

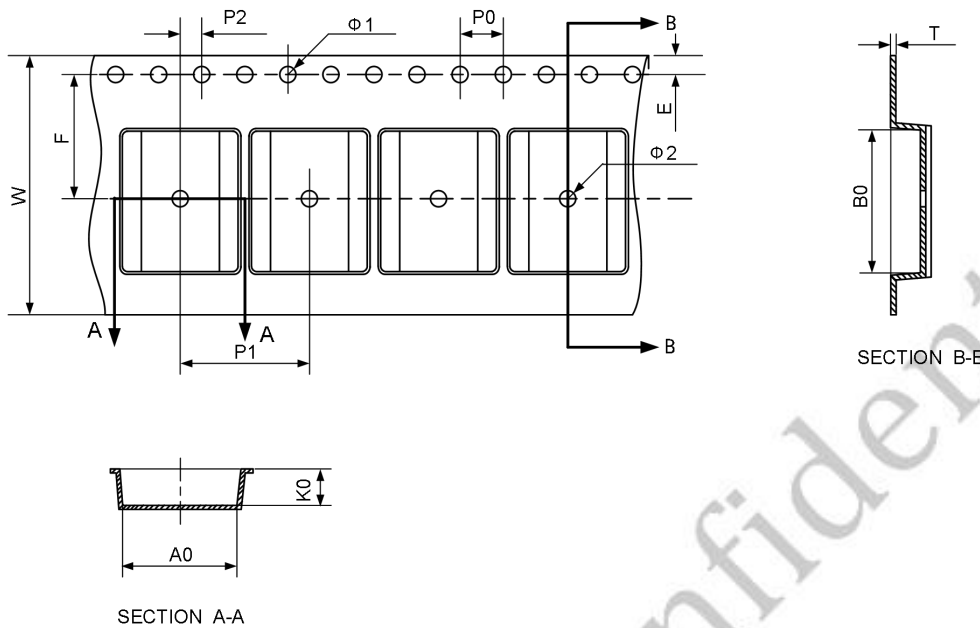
Output Voltage Detection

The JW7726HAE has output voltage detection function via VO pin. VCC is charged from VO pin when VO is higher than V_{O_EN} to save power loss caused by the LDO when charging from SW pin to VCC pin. When VO drops below V_{O_DIS} , the JW7726HAE is powered from SW pin.

TAPE AND REEL INFORMATION

Carrier Tape

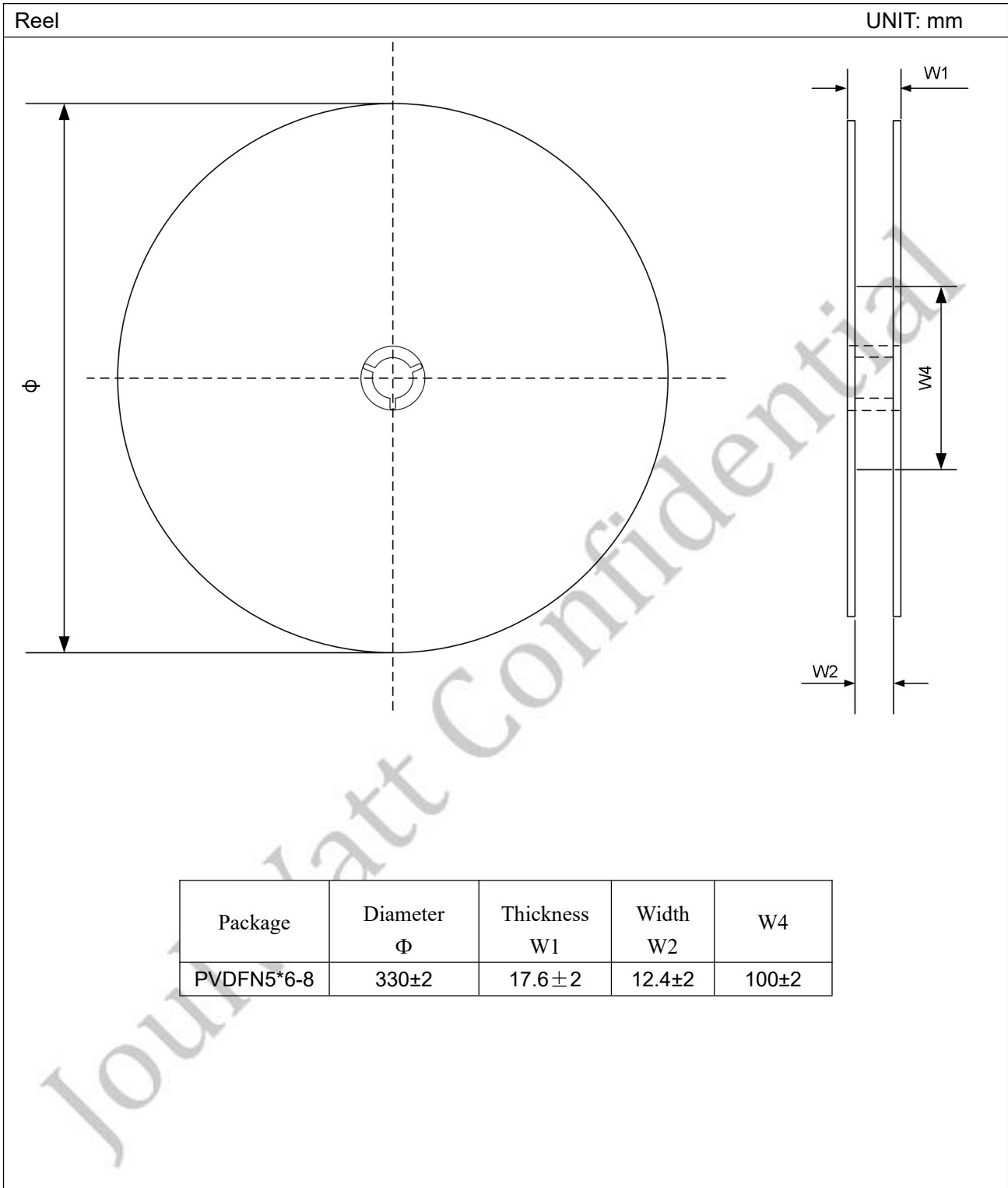
UNIT: mm



Note :

- 1) The carrier type is black, and colorless transparent.
- 2) Carrier camber is within 1mm in 100mm.
- 3) 10 pocket hole pitch cumulative tolerance:±0.20.
- 4) All dimensions are in mm.

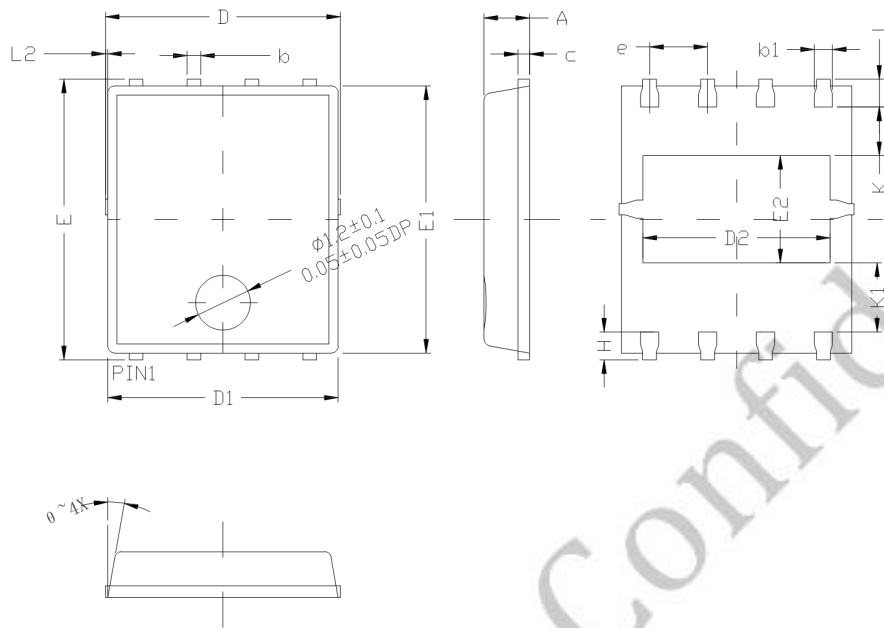
Package	Tape dimensions (mm)											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
PVDFN5*6-8	4.0±0.1	2.0±0.1	8.00±0.10	6.40±0.2	5.42±0.2	12.0±0.3	0.2±0.1	1.25±0.2	1.50min	1.50min	1.75±0.1	5.50±0.10



PACKAGE OUTLINE

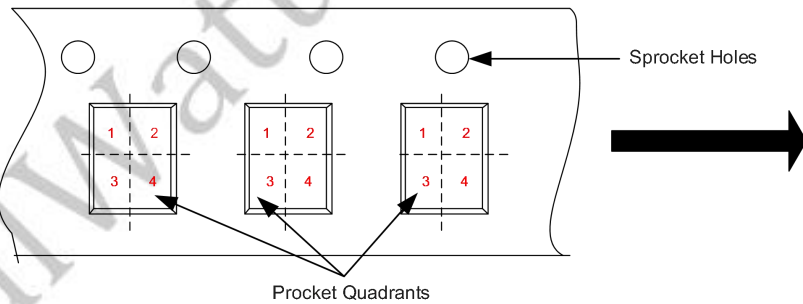
PVDFN5*6-8

UNIT: mm



SYM BDL	MILLIMETER		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.25	0.30	0.35
b1	0.30	0.40	0.45
c	0.22	0.25	0.28
D	--	--	5.30
D1	4.90	5.05	5.20
D2	4.10 REF		
E	6.00	6.15	6.30
E1	5.70	5.85	6.00
E2	2.35 REF		
e	1.10	1.27	1.40
H	0.51	0.61	0.71
K	1.00 REF		
K1	1.50 REF		
L	0.51	0.61	0.71
L2	--	--	0.10
theta	8°	~	12°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
PVDFN5*6-8	1

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